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JUL 3 1 2007 BY CARREST IN

Atty. Dkt. No. 047297-0137

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Hisatsugu KURITA et al.

Title:

SILICON WAFER CLEANING METHOD

Patent. No.:

7,226,513

Issue Date:

06/05/2007

Certificate

Examiner:

Michail Kornakov

AUG 0 2 2007

Art Unit:

1746

of Correction

Confirmation

8557

Number:

PTO MISTAKE PURSUANT TO 37 C.F.R. § 1.322(a)

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

Enclosed, in duplicate, is a Certificate of Correction, Form PTO-SB/44, for United States Patent Number 7,226,513 issued June 5, 2007. The following Patent Office printing errors appear in the issued patent:

IN THE SPECIFICATION

The exact column and line number where the error in the issued patent is shown correctly in the application are:

Column 10, line 1 should reads as "oxidizing a silicon wafer annealed under", Please delete the second occurrence of "a silicon wafer".

Applicant submits that the above changes would not constitute new matter, and correction thereof would not require reexamination.

Pursuant to 37 C.F.R. §1.322, Applicant requests that the enclosed Certificate of Correction be approved.

Although Applicant believes that no fee is required for this Request, the Commissioner is hereby authorized to charge any additional fees which may be required for this Request to Deposit Account No. 19-0741.

Respectfully submitted,

Date _____ JUL 3 1 2007

T.

FOLEY & LARDNER LLP Customer Number: 22428

Telephone: (202) 672-5414 Facsimile: (202) 672-5399 Richard L. Schwaab Attorney for Applicant Registration No. 25,479 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO.

7,226,513

APPLICATION NO.

10/645,911

DATED

06/05/2007

INVENTOR(S)

Hisatsugu KURITA; Manabu HIRASAWA; Hiromi NAGAHAMA;

Koji IZUMOME; Takao INO; Jyunsei YAMABE; Naoya HAYAMIZU;

Naoaki SAKURAI

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 10, line 1 should reads as "oxidizing a silicon wafer annealed under"

MAILING ADDRESS OF SENDER (Please do not use customer number below):

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